IN THE CLAIMS:

1. (Currently Amended) A circuit for recovering a clock signal in a USB (universal serial bus) receiver, the circuit comprising:

a phase detector for detecting a phase difference between data received from a USB transmitter and a recovery clock signal and generating a first control signal indicative of a detected phase difference;

a bidirectional shift register for outputting a second control signal in response to the first control signal;

a multiphase clock signal generator for processing a receiver clock signal of the USB receiver, wherein the receiver clock signal is the same as a transmitter clock signal of the USB transmitter, to generate a plurality of phase clock signals each having the same frequency as the receiver clock signal and a different phase offset from the phase of the receiver clock signal; and

a phase selector responsive to the second control signal for selecting one of the plurality of phase clock signals and outputting the selected phase clock signal as a recovery clock signal,

wherein the plurality of phase clock signals comprise first through N-th phase clock signals, wherein the different phase offsets of the first through N-th phase clock signals are about (360/N)I degrees, where N is an integer, and I is an integer equal to or greater than 0 and equal to or less than N-1.

2. (Canceled)

3. (Currently Amended) The circuit of claim [2] 1, wherein N is an integer equal to or greater than 2 and equal to or less than 8.

4. (Currently Amended) The circuit of claim [2] 1, wherein N is 8.

5. (Original) The circuit of claim 1, wherein the bidirectional shift register is shifted in a first direction when the first control signal is at a first predetermined level, and shifted in a second direction when the first control signal is at a second predetermined level.

6. (Original) The circuit of claim 1, wherein the multiphase clock signal generator comprises a multiphase analog PLL (phase locked loop) circuit.

7. (Original) The circuit of claim 1, further comprising a clock signal generator for generating the receiver clock signal.

8. (Original) The circuit according to claim 7, wherein the clock signal generator comprises:

a crystal oscillator for generating a clock signal having a predetermined frequency; and

a frequency multiplier for multiplying the frequency of the clock signal to generate the receiver clock signal.

9. (Currently Amended) A method for recovering a clock signal in a USB (universal serial bus) receiver, the method comprising the steps of:

receiving a receiver clock signal of the USB receiver having a frequency equal to the frequency of a transmitter clock signal of a USB transmitter, and generating a plurality of phase clock signals from the receiver clock signal, wherein each phase clock signal has the same

frequency as the receiver clock signal and a different phase offset from the phase of the receiver clock signal;

detecting a phase difference between data received from a USB transmitter and a recovery clock signal and generating a first control signal indicative of a detected phase difference;

outputting a second control signal from a bidirectional shift register in response to the first control signal; and

selecting one of the plurality of phase clock signals in response to the second control signal and outputting the selected phase clock signal as a recovery clock signal,

wherein the step of generating a plurality of phase clock signals comprises the step of generating first through N-th phase clock signals, wherein the different phase offsets of the first through N-th phase clock signals are about (360/N)I degrees, where N is an integer, and I is an integer equal to or greater than 0 and equal to or less than N-1.

10. (Canceled)

11. (Currently Amended) The method of claim [10] 9, wherein N is an integer equal to or greater than 2 and equal to or less than 8.

12. (Currently Amended) The method of claim [10] 9, wherein N is 8.

13. (Currently Amended) A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for recovering a clock signal in a communications system comprising a transmitter and receiver, the method steps comprising:

receiving a receiver clock signal of the receiver having a frequency equal to the frequency of a transmitter clock signal of the transmitter, and generating a plurality of phase clock signals from the receiver clock signal, wherein each phase clock signal has the same frequency as the receiver clock signal and a different phase offset from the phase of the receiver clock signal;

detecting a phase difference between data received from the transmitter and a recovery clock signal and generating a first control signal indicative of a detected phase difference;

outputting a second control signal from a bidirectional shift register in response to the first control signal; and

selecting one of the plurality of phase clock signals in response to the second control signal and outputting the selected phase clock signal as a recovery clock signal,

wherein the instructions for generating a plurality of phase clock signals comprise instructions for generating first through N-th phase clock signals, wherein the different phase offsets of the first through N-th phase clock signals are about (360/N)I degrees, where N is an integer, and I is an integer equal to or greater than 0 and equal to or less than N-1.

14. (Canceled)

15. (Original) The program storage device of claim 13, wherein the method steps are implemented in a USB (universal serial bus) communications system.

16. (Currently Amended) A communications system, comprising:

a transmitter; and

a receiver comprising means for recovering a clock signal, wherein the means for recovering a clock signal comprises:

phase detecting means for detecting a phase difference between data received from the transmitter and a recovery clock signal and generating a first control signal indicative of a detected phase difference;

bidirectional shift register means for outputting a second control signal in response to the first control signal;

multiphase clock signal generating means for generating a plurality of phase clock signals each having the same frequency as a receiver clock signal of the receiver and a different phase offset from the phase of the receiver clock signal; and

selecting means responsive to the second control signal for selecting one of the plurality of phase clock signals and outputting the selected phase clock signal as a recovery clock signal,

wherein the plurality of phase clock signals comprise first through N-th phase clock signals, wherein the different phase offsets of the first through N-th phase clock signals are about (360/N)I degrees, where N is an integer, and I is an integer equal to or greater than 0 and equal to or less than N-1.

17. (Original) The system of claim 16, wherein the communications system comprises a USB (universal serial bus) communications system.

18. (Canceled)

19. (Currently Amended) The system of claim [18] 16, wherein N is an integer equal to or greater than 2 and equal to or less than 8.

20. (Currently Amended) The system of claim [18] 16, wherein N is 8.